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(54) **ORGANIC LIGHT EMITTING DISPLAY DEVICE AND METHOD FOR FABRICATING THE SAME**

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(57) **ABSTRACT**

An organic light emitting display device including a thin film transistor in first and second regions on a transparent insulating substrate, a lower anode coupled to the thin film transistor, a reflective layer pattern formed on the lower anode in the first region, an upper anode formed on the reflective layer pattern in the first region and on the lower anode in the second region, and an organic layer formed on the upper anode in the first and second regions.

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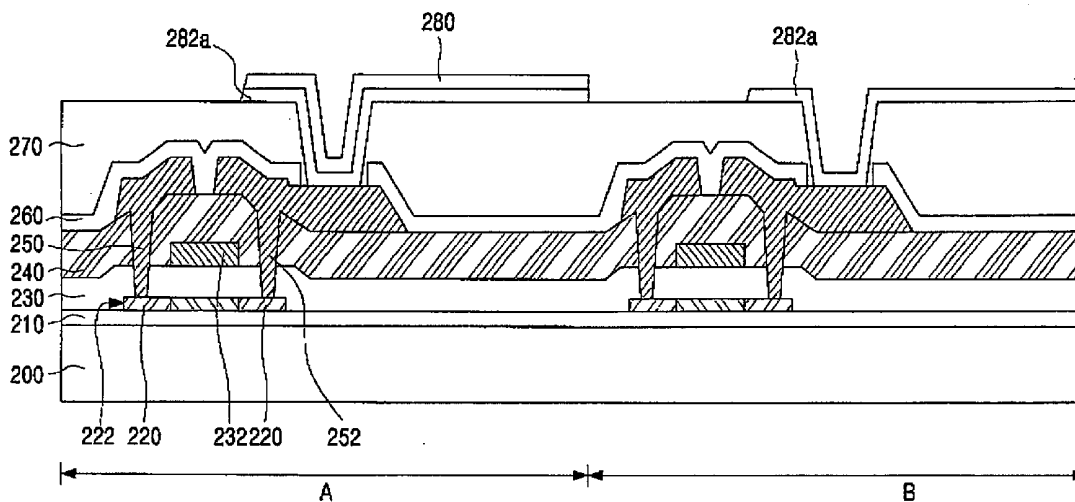


FIG. 1A
(PRIOR ART)

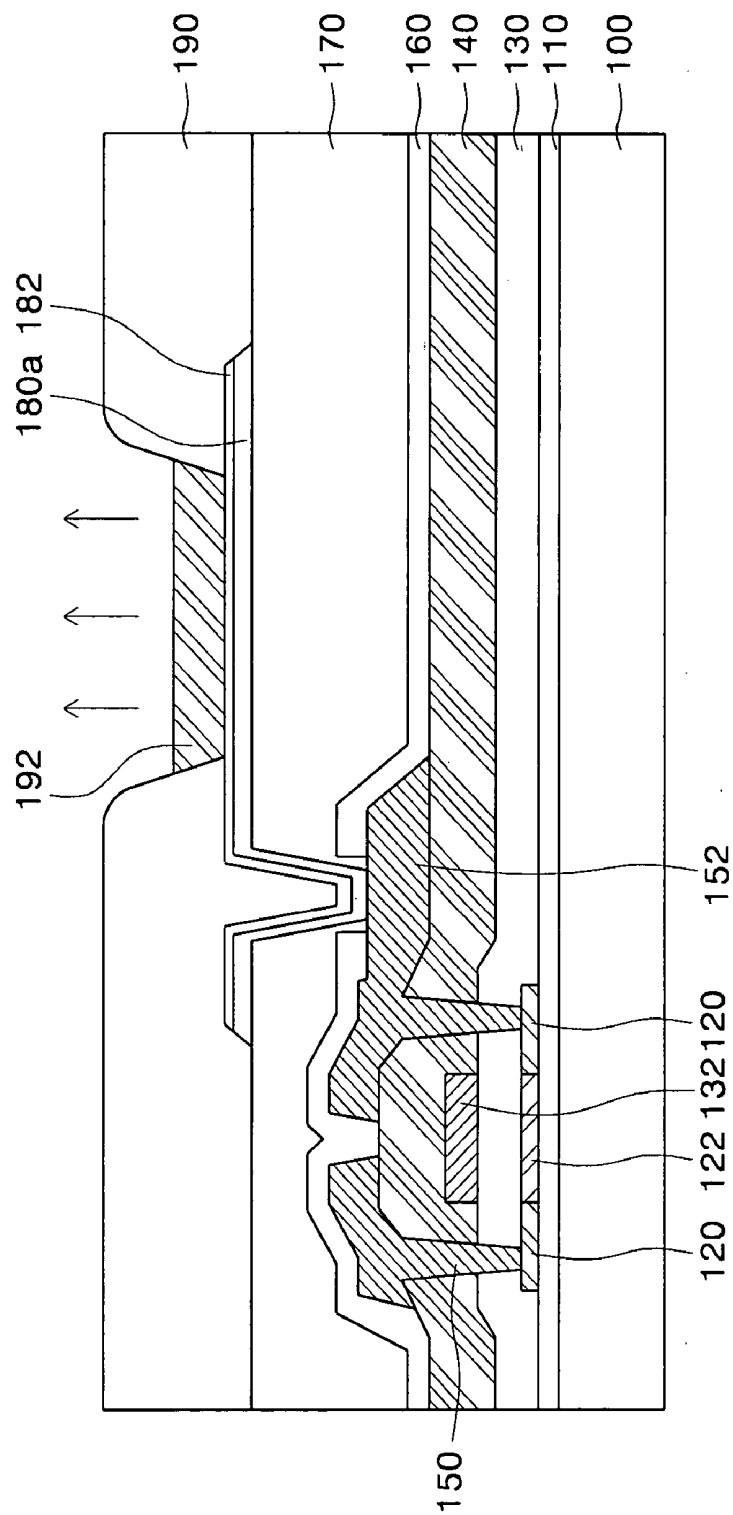


FIG. 1B
(PRIOR ART)

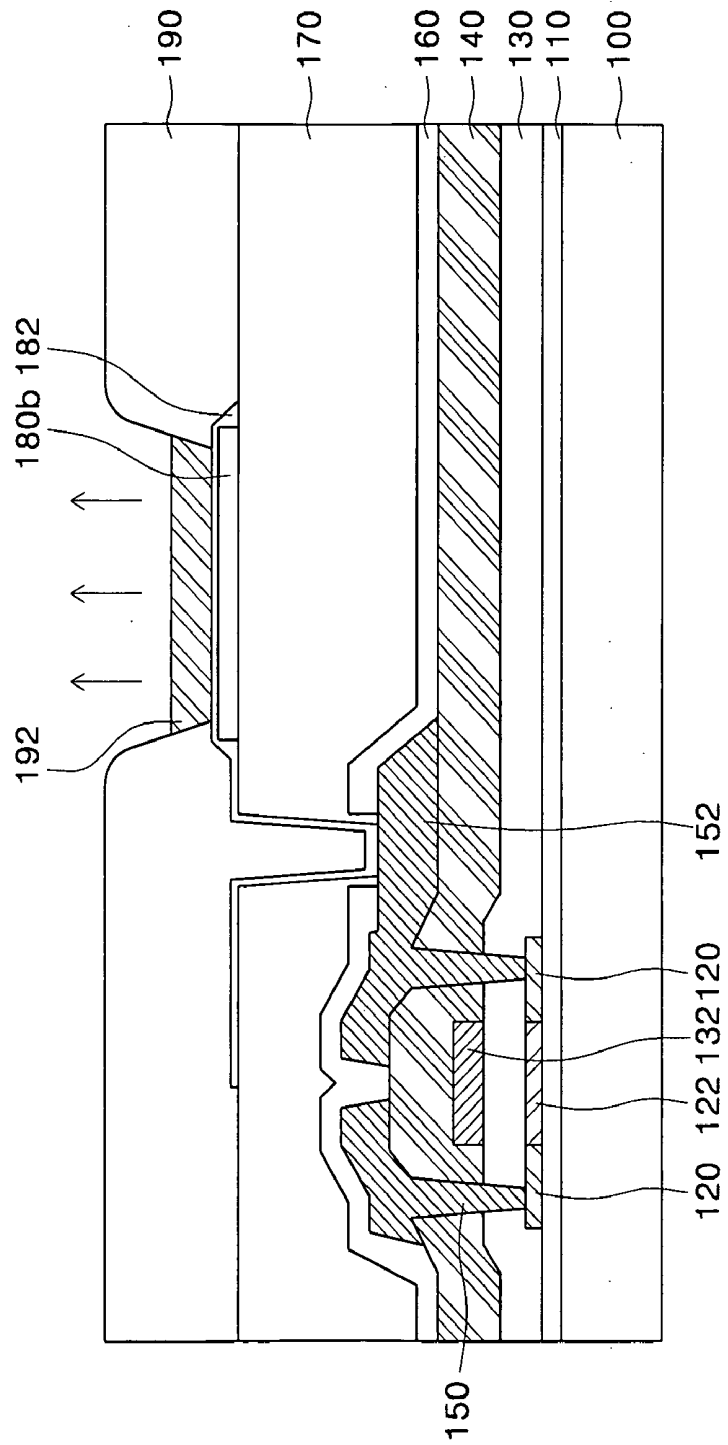


FIG. 2A

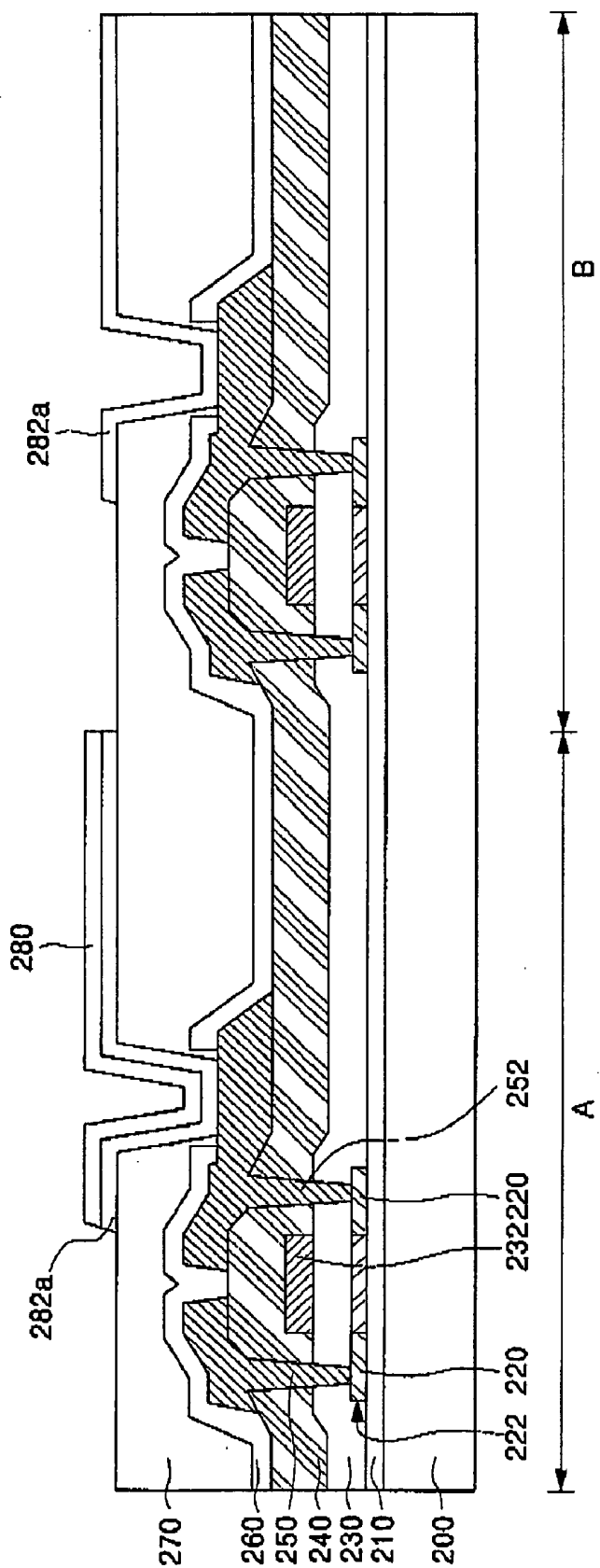


FIG. 2B

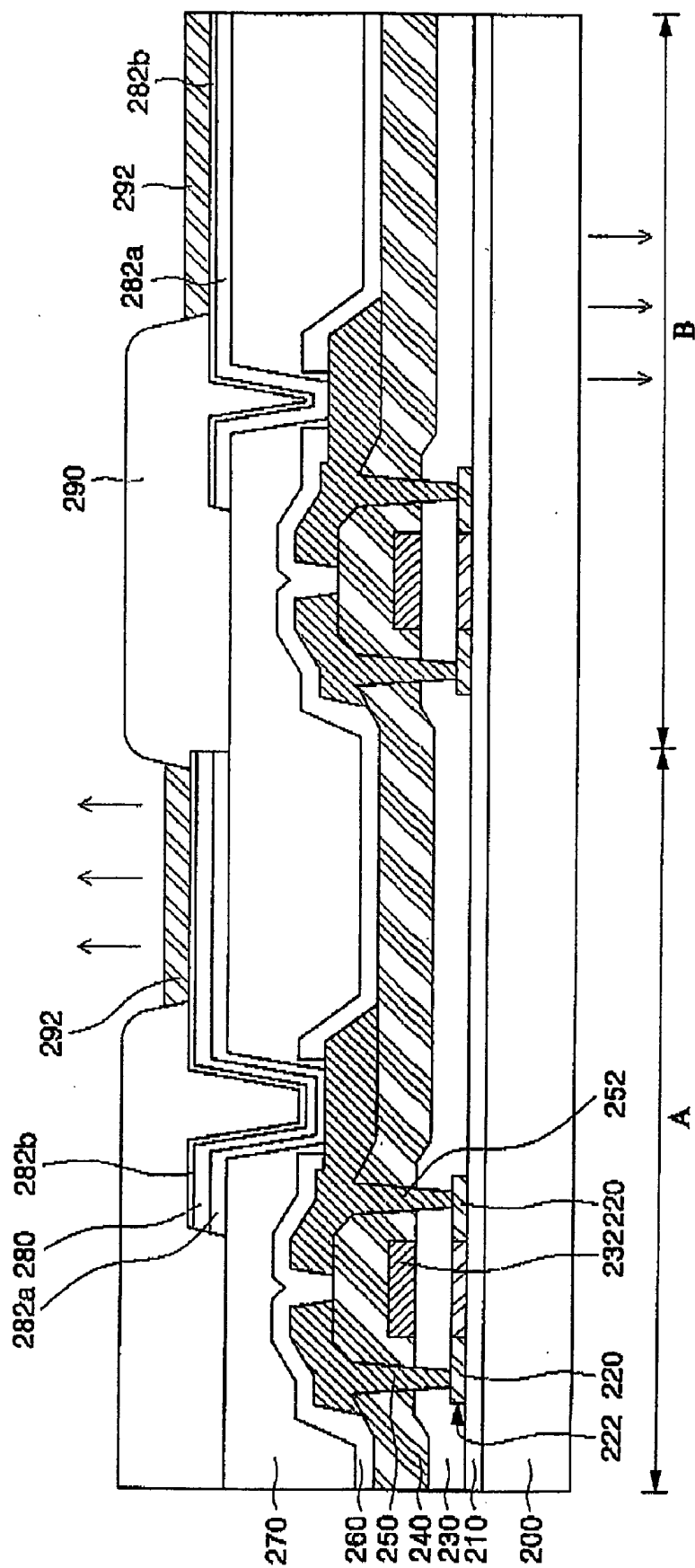


FIG. 3

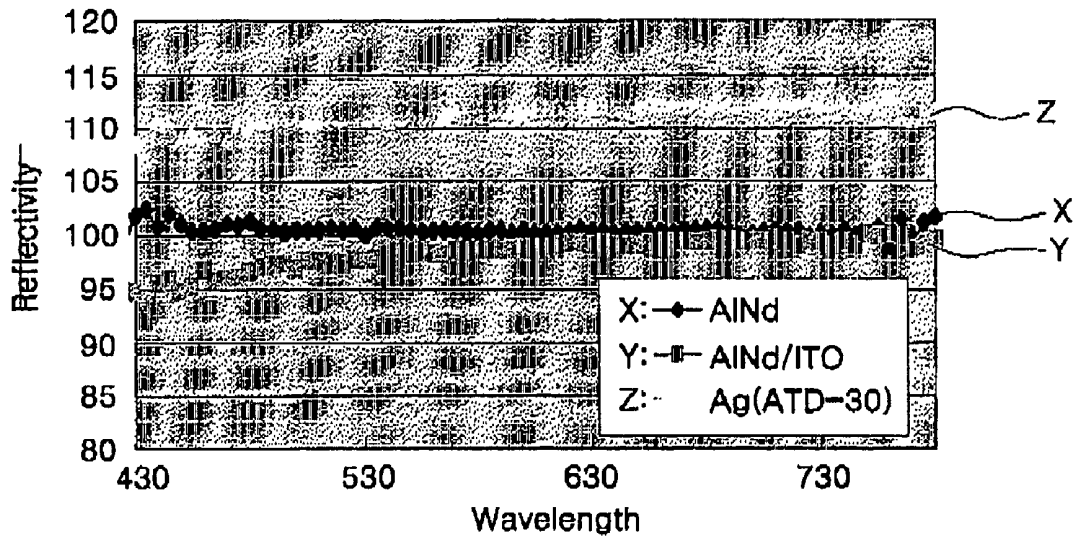
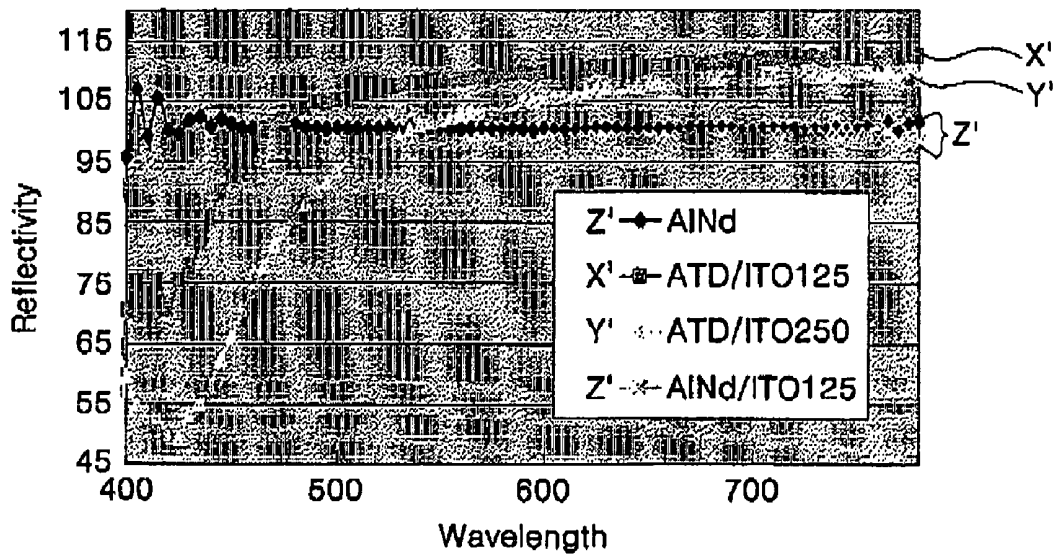


FIG. 4



ORGANIC LIGHT EMITTING DISPLAY DEVICE AND METHOD FOR FABRICATING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2004-0038535, filed May 28, 2004, which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to an organic light emitting display (OLED) device and method for fabricating the same and, more particularly, to an OLED device having anode layers with a reflective layer interposed therebetween and method for fabricating the same.

[0004] 2. Discussion of the Background

[0005] Generally, an OLED device is an emissive display device that emits light by electrically exciting fluorescent organic compounds. An OLED device may be considered a passive matrix OLED (PMOLED) device or an active matrix OLED (AMOLED) device depending on a manner of driving $N \times M$ pixels, which may be arranged in a matrix. The AMOLED device is suitable for large displays because of its low power consumption and high resolution, as compared to the PMOLED device.

[0006] Depending on a direction which light emits from the organic compound, an OLED device may be a top-emitting OLED device, a bottom-emitting OLED device, or a top and bottom-emitting OLED device. The top-emitting OLED device emits light in an opposite direction of a substrate with the pixels positioned thereon and it may have a high aperture ratio, unlike the bottom-emitting OLED.

[0007] Demand is increasing for an OLED device comprising both a top-emitting type, for a primary display window, and a bottom-emitting type, for a secondary display window, because the device may be miniaturized and it may consume little power. Such an OLED device may be primarily used for a portable telephone including the secondary display window outside and the primary display window therein. The secondary display window consumes less power than the primary display window, and it may remain on when the portable telephone is in a call waiting state, thus allowing a reception state, battery remaining amount, time, and the like to be observed at any time.

[0008] FIG. 1A is a cross-sectional view showing a conventional OLED device.

[0009] First, a buffer layer 110 is formed to a predetermined thickness on a transparent insulating substrate 100, and a thin film transistor, which includes a polycrystalline silicon pattern 122, a gate electrode 132, and source and drain electrodes 150 and 152, is formed on the substrate. Source and drain regions 120, having implanted impurities, are formed at both sides of the polycrystalline silicon pattern 122. A gate insulating layer 130 is formed on the entire surface of the substrate including the polycrystalline silicon pattern 122. The source and drain electrodes 150 and 152 are formed on an interlayer insulating layer 140, and they are connected to the source and drain regions 120 through contact holes.

[0010] A passivation layer 160 is then formed to a predetermined thickness on the entire surface and etched by photolithography and etching processes to form a first via contact hole (not shown) exposing either the source or drain electrode 150 or 152. FIG. 1A shows the exposed drain electrode 152. The passivation layer 160 is an inorganic insulating layer, which may comprise a silicon nitride layer, a silicon oxide layer, or a stacked structure thereof.

[0011] Next, a first insulating layer 170 is formed on the entire surface of the substrate. It may be formed of one material selected from a group consisting of polyimide, benzocyclobutene series resin, spin on glass (SOG), and acrylate. The first insulating layer 170 is formed to planarize a pixel region.

[0012] The first insulating layer 170 is subsequently etched by photolithography and etching processes to form a second via contact hole (not shown) exposing the first via contact hole.

[0013] Next, a stacked structure of a reflective layer (not shown) and a thin layer (not shown) for an anode is formed on the entire surface. The reflective layer may be formed of a metal having high reflectivity, such as aluminum (Al), molybdenum (Mo), titanium (Ti), gold (Au), silver (Ag), palladium (Pd), an alloy of these metals, or the like. Forming the reflective layer described above provides a top-emitting OLED device. On the other hand, forming the reflective layer in a subsequent process provides a bottom-emitting OLED device.

[0014] The thin layer for the anode is formed about 10 to 300 Å thick using a transparent metal material, such as Indium Tin Oxide (ITO).

[0015] The stacked structure is subsequently etched by photolithography and etching processes to form an anode 182 and a reflective layer pattern 180a.

[0016] A second insulating layer pattern 190 defining an emission region may then be formed on the entire surface of the substrate. The second insulating layer pattern 190 may be formed of one material selected from the group consisting of polyimide, benzocyclobutene series resin, phenol resin, and acrylate.

[0017] Subsequently, an emission layer 192 is formed in the emission region defined by the second insulating layer pattern 190, using a small molecule deposition method or a laser induced thermal imaging method. A cathode (not shown) and the like are then formed to thereby complete the OLED device. When forming a top-emitting OLED device, the cathode is formed of a transparent electrode or a transparent metal electrode, and when forming a bottom-emitting OLED device, the cathode is formed of a metal electrode having a reflective layer, or a reflective electrode.

[0018] If the reflective layer pattern and the anode in the top-emitting OLED device are formed in the stacked structure as described above, they may be simultaneously exposed to an electrolyte solution that is used in the photolithography and etching processes, in which may damage the anode. Such damage may degrade the device's optical properties, such as brightness.

[0019] FIG. 1B is a cross-sectional view showing another conventional OLED device. The OLED device of FIG. 1B may form a reflective layer pattern 180b in an island

structure to solve the above problem. This may prevent the reflective layer pattern **180b** and the anode **182** from being simultaneously exposed to the electrolyte solution.

[0020] Since the top-emitting OLED device uses a resonance effect of light as described above, forming the anode as thin as possible facilitates color-coordinates adjustment. However, forming the thin anode may cause a short circuit at a step of the via contact hole. Further, when fabricating the OLED device including both the top-emitting OLED device and the bottom-emitting OLED device, using equally thick anodes for the top and bottom-emitting OLED devices may degrade the device's optical properties due to an increase in resistance.

SUMMARY OF THE INVENTION

[0021] The present invention provides an OLED device, and method for fabricating the same, having improved reliability by including a first region having a stacked structure of a lower anode, a reflective layer pattern with silver, and an upper anode, and a second region having a stacked structure of a lower anode and an upper anode.

[0022] Additional features of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention.

[0023] The present invention discloses an OLED device including a thin film transistor in first and second regions on a transparent substrate, and a lower anode coupled to either a source or drain electrode of the thin film transistor in the first and second regions. A reflective layer pattern is formed on the lower anode in the first region, and an upper anode is formed on the reflective layer pattern in the first region and on the lower anode in the second region. An organic layer is formed on the upper anode in the first and second regions.

[0024] The present invention also discloses a method of fabricating an OLED device including forming a thin film transistor in a first region and a second region on a transparent substrate, forming a lower anode coupled to either a source or drain electrode of the thin film transistor in the first and second regions. A reflective layer pattern is formed on the lower anode in the first region, and an upper anode is formed on the reflective layer pattern in the first region and on the lower anode in the second region. An organic layer, having at least an emission layer, is formed on the upper anode in the first and second regions.

[0025] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0027] FIG. 1A is a cross-sectional view showing a conventional OLED device.

[0028] FIG. 1B is a cross-sectional view showing a conventional OLED device.

[0029] FIG. 2A and FIG. 2B are cross-sectional views showing a method of fabricating an OLED device according to an exemplary embodiment of the present invention.

[0030] FIG. 3 is a graph showing reflectivity depending on the type of a reflective layer.

[0031] FIG. 4 is a graph showing reflectivity depending on the type of a reflective layer and anode thickness.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0032] Hereinafter, exemplary embodiments of the present invention will be described with reference to the accompanying drawings.

[0033] FIG. 2A and FIG. 2B are cross-sectional views showing an OLED device according to an exemplary embodiment of the present invention. Referring to FIG. 2A and FIG. 2B, a transparent insulating substrate **200** comprises a first region A and a second region B having differently structured anodes.

[0034] The anode in the first region A may have a stacked structure including a lower anode **282a**, a reflective layer pattern **280** formed on the entire surface of the lower anode **282a**, and an upper anode **282b** formed on the reflective layer pattern **280**. The lower anode **282a** may be thicker than the upper anode **282b**, and the reflective layer pattern **280** may be formed of silver (Ag) on the same region as the lower anode **282a** and the upper anode **282b**.

[0035] The anode in the second region B may have a stacked structure including the lower anode **282a** and the upper anode **282b**. The lower anode **282a** may be formed to such a thickness that does not degrade optical properties even in increased resistance.

[0036] An OLED device according to an exemplary embodiment of the present invention may be formed by the following method.

[0037] The first region A and the second region B may be first defined on the transparent insulating substrate **200**, which may be made of glass, quartz, sapphire, or other similar materials. All subsequent processes, except the process of forming the reflective layer in the first region A, may be simultaneously carried out in the first region A and the second region B.

[0038] Next, a buffer layer **210**, which may be made of silicon oxide, may be formed to a predetermined thickness on the entire surface of the transparent insulating substrate **200** by a plasma-enhanced chemical vapor deposition (PECVD) method or other like method. The buffer layer **210** prevents diffusion of impurities in the transparent insulating substrate **200** when crystallizing a subsequently formed amorphous silicon layer.

[0039] The amorphous silicon layer (not shown) may then be deposited to a predetermined thickness on the buffer layer **210** and crystallized by excimer laser annealing (ELA), sequential lateral solidification (SLS), metal induced crystallization (MIC), metal induced lateral crystallization (MILC), or other similar methods. Thereafter, a polycrystalline silicon pattern **222** may be formed in the thin film

transistor region within the unit pixel by patterning using photolithography and etching processes. The polycrystalline silicon pattern **222** also includes subsequently formed source and drain regions **220**.

[0040] Next, a gate insulating layer **230** may be formed to a predetermined thickness on the entire surface of the substrate. The gate insulating layer **230** may be formed of silicon oxide, silicon nitride, a stacked structure thereof, or other like materials.

[0041] A metal layer (not shown), which forms a gate electrode, may be formed on the gate insulating layer **230**. The metal layer may be a single layer of aluminum (Al) or an aluminum alloy such as aluminum-neodymium (AlNd), or it may be a multilayer in which the aluminum alloy is stacked on chromium (Cr) or molybdenum (Mo) alloy. The metal layer may then be etched by photolithography and etching processes to form a gate electrode **232**. Thereafter, impurity ions may be injected into the polycrystalline silicon pattern **222** on both sides of the gate electrode **232**, thereby forming the source and drain regions **220**.

[0042] Next, an interlayer insulating layer **240** may be formed to a predetermined thickness on the entire surface of the substrate. A silicon nitride layer, or other like materials, may be used for the interlayer insulating layer **240**.

[0043] The interlayer insulating layer **240** and the gate insulating layer **230** may then be etched by photolithography and etching processes, thereby forming a contact hole (not shown) exposing the source and drain regions **220**. An electrode material may be formed on the entire surface of the substrate including the contact hole and etched by photolithography and etching processes, thereby forming source and drain electrodes **250** and **252**, which are coupled to the source and drain regions **220**. Molybdenum-tungsten (MoW), aluminum-neodymium (AlNd), a stacked structure thereof, or other like materials may be used for the electrode material.

[0044] Next, a passivation layer **260** may be formed to a predetermined thickness on the entire surface of the substrate by depositing a silicon nitride layer, a silicon oxide layer, a stacked structure thereof, or other like materials.

[0045] The passivation layer **260** may then be etched by photolithography and etching processes, thereby forming a first via contact hole (not shown) exposing either the source or drain electrode **250**, **252**. FIG. 2B shows the drain electrode **252** exposed.

[0046] A first insulating layer **270** may be formed on the entire surface of the substrate at a thickness that fully planarizes the thin film transistor region. The first insulating layer **270** may be formed of one material selected from the group consisting of polyimide, benzocyclobutene series resin, spin on glass (SOG), and acrylate.

[0047] Next, the first insulating layer **270** is etched by photolithography and etching processes, thereby forming a second via contact hole (not shown) exposing either the source or drain electrode **250**, **252** exposed by the first via contact hole.

[0048] A thin layer for a lower anode (not shown) may then be formed on the entire surface of the substrate. The thin layer for the lower anode may be about a 100 to 1000 Å thick transparent metal electrode, such as ITO, IZO,

In_2O_3 , or Sn_2O_3 . This thin layer may improve interfacial properties, namely, the adhesive properties between the reflective layer and the first insulating layer **270** in the first region, and may prevent resistance from increasing in the second region.

[0049] Next, the thin layer for the lower anode may be etched by photolithography and etching processes, thereby forming a lower anode **282a**. The lower anode **282a** may be coupled to either the source or drain electrode **250**, **252**. FIG. 2B shows the lower anode **282a** coupled to the drain electrode **252** through the second via contact hole.

[0050] A reflective layer (not shown) may then be formed on the entire surface substrate. The reflective layer may be formed of silver (Ag), palladium (Pd) or platinum (Pt), or other like materials, having greater than 80% reflectivity. The reflective layer is preferably formed of silver (Ag), and it may be formed about 500 to 3000 Å thick.

[0051] Next, the reflective layer may be etched by photolithography and etching processes, thereby forming a reflective layer pattern **280** on a surface of the lower anode **282a** in the first region A. The reflective layer pattern **280** may increase brightness and luminous efficiency by acting as a light reflector in the first region A. As FIG. 2A and FIG. 2B show, the reflective layer pattern **280** is not formed in the second region B.

[0052] A thin layer for an upper anode (not shown) may then be formed on the entire surface of the substrate. The thin layer for the upper anode may be about 10 to 300 Å thick. Preferably, it is about 20 to 100 Å thick, thus facilitating color-coordinate adjustment.

[0053] Next, the thin layer for the upper anode may be etched by photolithography and etching processes, thereby forming an upper anode **282b**. The upper anode **282b** may be formed on and at a side of the reflective layer pattern **280** in the first region A, and it may be formed on the lower anode **282a** in the second region B. Hence, the anode in the first region A may comprise a triple layered structure of the lower anode **282a**, the reflective layer pattern **280**, and the upper anode **282b**, while the anode in the second region B may comprise a double layered structure of the lower anode **282a** and the upper anode **282b**.

[0054] A second insulating layer (not shown) may then be formed on the entire surface of the substrate.

[0055] Next, a second insulating layer pattern **290**, which defines an emission region, may be formed by etching the second insulating layer using photolithography and etching processes.

[0056] An emission layer **292** may then be formed in the emission region exposed by the second insulating layer pattern **290** by a small molecular deposition method, a laser thermal transfer method, or other like methods. The emission layer **292** may comprise at least one of an electron injecting layer, an electron transporting layer, a hole injecting layer, a hole transporting layer, a hole blocking layer, and an organic emission layer.

[0057] Although not shown, a cathode may then be formed to complete the OLED device. The cathode in the first region A may be a transparent electrode or transparent metal electrode, while the cathode in the second region B may be a transparent electrode having a reflective layer

stacked thereon, or a reflective electrode. The cathode in the second region B may also be formed of a transparent electrode or a transparent metal electrode, like the cathode in the first region A.

[0058] FIG. 3 is a graph showing reflectivity versus light wavelength depending on the type of a reflective layer. AlNd is used for the reflective layer in case (X), ITO is formed on the AlNd as the reflective layer in case (Y), and silver (Ag) is used for the reflective layer in case (Z). In case (Z), where the silver (Ag) is used for the reflective layer, a silver alloy ATD-30 (product name) was used for the silver (Ag). FIG. 3 shows that, irrespective of the wavelength of the light, the reflectivity in case (Z), where the silver (Ag) is used for the reflective layer, is about 15% higher than cases (X) and (Y), where AlNd and ITO formed on AlNd, are used as the reflective layer, respectively.

[0059] FIG. 4 is a graph showing a reflectivity versus light wavelength depending on the type of a reflective layer and the thickness of the anode layer formed on the reflective layer. Silver (Ag) is used for the reflective layer in cases (X' and Y'), and AlNd is used for the reflective layer in case Z'. The anode layer formed on the silver (Ag) reflective layer is about 125 Å thick in case (X') and about 250 Å thick in case (Y'). If the anode formed on the reflective layer is about 250 Å thick, reflectivity is dramatically degraded in a short wavelength region where the wavelength of the light is equal to or less than about 500. Therefore, when using silver (Ag) for the reflective layer, the thinner the anode formed on the reflective layer, the less the reflectivity changes depending on the wavelength of the light.

[0060] As described above, interposing a reflective layer pattern between two anode layers may improve reflectivity, prevent resistance in the junction region of the anodes from increasing, and prevent a short circuit from occurring between the anodes at a step portion, thereby improving the device's properties and reliability.

[0061] It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. An organic light emitting display device, comprising:
 - a thin film transistor in a first region and a second region on a transparent substrate;
 - a lower anode coupled to either a source electrode or a drain electrode of the thin film transistor in the first region and the second region;
 - a reflective layer pattern formed on the lower anode in the first region;
 - an upper anode formed on the reflective layer pattern in the first region and the lower anode in the second region; and
 - an organic layer formed on the upper anode in the first region and the second region and having at least an emission layer.

2. The device of claim 1, further comprising:

an insulating layer,

wherein the lower anode is coupled to the source electrode or the drain electrode through a contact hole in the insulating layer; and

wherein the insulating layer comprises a stacked structure of a passivation layer and a planarization layer.

3. The device of claim 1, further comprising:

an insulating layer,

wherein the lower anode is coupled to the source electrode or the drain electrode through a contact hole in the insulating layer; and

wherein the insulating layer is a stacked structure of an inorganic insulating layer and an organic insulating layer.

4. The device of claim 1, wherein the lower anode is about 100 to 1 to 1000 Å thick.

5. The device of claim 1, wherein the reflective layer pattern is formed of one of silver, platinum, or palladium.

6. The device of claim 5, wherein the reflective layer pattern is formed of silver.

7. The device of claim 1, wherein the reflective layer pattern is about 500 to 3000 Å thick.

8. The device of claim 1, wherein the upper anode is about 10 to 300 Å thick.

9. The device of claim 8, wherein the upper anode is about 20 to 1 to 100 Å thick.

10. The device of claim 1, further comprising:

a cathode formed on the organic layer in the first region and the second region,

wherein the cathode in the first region is a transparent electrode; and

wherein the cathode in the second region is either a transparent electrode or a reflective electrode.

11. A method for fabricating an organic light emitting display device, comprising:

forming a thin film transistor in a first region and a second region of a transparent substrate;

forming a lower anode coupled to either a source electrode or a drain electrode of the thin film transistor in the first region and the second region;

forming a reflective layer pattern on the lower anode in the first region;

forming an upper anode on the reflective layer pattern in the first region and on the lower anode in the second region; and

forming an organic layer having at least an emission layer on the upper anode in the first region and the second region.

12. The method of claim 11, further comprising:

forming an insulating layer in a stacked structure of a passivation layer and a planarization layer; and

forming a contact hole in the insulating layer in the first region and the second region,

wherein the lower anode is coupled to the source electrode or the drain electrode through the contact hole in the insulating layer.

13. The method of claim 11, further comprising:

forming an insulating layer in a stacked structure of an inorganic insulating layer and an organic insulating layer; and

forming a contact hole in the insulating layer in the first region and the second region,

wherein the lower anode is coupled to the source electrode or the drain electrode through the contact hole in the insulating layer.

14. The method of claim 12, wherein forming the contact hole in the insulating layer in the first region and the second region comprises performing two photolithography and etching processes.

15. The method of claim 13, wherein forming the contact hole in the insulating layer in the first region and the second region comprises performing two photolithography and etching processes.

16. The method of claim 11, wherein the lower anode is formed to be about 100 to 1000 Å thick.

17. The method of claim 11, wherein the reflective layer pattern is formed of one of silver, platinum, or palladium.

18. The method of claim 17, wherein the reflective layer pattern is formed of silver.

19. The method of claim 11, wherein the reflective layer pattern is formed to be about 500 to 3000 Å thick.

20. The method of claim 11, wherein the upper anode is formed to be about 10 to 300 Å thick.

21. The method of claim 20, wherein the upper anode is formed to be about 20 to 100 Å thick.

22. The method of claim 11, further comprising:

forming a cathode on the organic layer in the first region and the second region,

wherein the cathode in the first region is formed of a transparent electrode; and

wherein the cathode in the second region is formed of either a transparent electrode or a reflective electrode.

* * * * *

专利名称(译)	有机发光显示装置及其制造方法		
公开(公告)号	US20050264183A1	公开(公告)日	2005-12-01
申请号	US11/126341	申请日	2005-05-11
[标]申请(专利权)人(译)	SEO张苏 姜泰旭 公园文熙		
申请(专利权)人(译)	SEO CHANG-SU KANG TAE 旭 PARK 文姬		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	SEO CHANG SU KANG TAE WOOK PARK MOON HEE		
发明人	SEO, CHANG-SU KANG, TAE-WOOK PARK, MOON-HEE		
IPC分类号	H05B33/26 H01J1/62 H01J63/04 H01L27/32 H01L51/52 H05B33/14		
CPC分类号	H01L27/3258 H01L27/3267 H01L2251/558 H01L51/5234 H01L51/5218		
优先权	1020040038535 2004-05-28 KR		
其他公开文献	US7687984		
外部链接	Espacenet USPTO		

摘要(译)

一种有机发光显示装置，包括在透明绝缘基板上的第一和第二区域中的薄膜晶体管，连接到薄膜晶体管的阳极，形成在第一区域中的下阳极上的反射层图案，形成的上阳极在第一区域中的反射层图案和第二区域中的下阳极上，以及在第一和第二区域中的上阳极上形成的有机层。

